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Safety in Operation Logic – FPGA Approach

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Abstract— Manual Safety Logic Unit implements the interlocks using Field Programmable Gate Array (FPGA) for safe operation of Fuel Handling components of Advanced Heavy Water Reactor (AHWR). The interlocks have been designed to prevent any mal-operation and damage to the fueling components. Interlocks are the instrumented functions and the interconnections between them are determined by the user. This paper summarizes the safety operation of Fueling Machine component i.e. RAM Assembly by checking the output commands given by Control Computer after verifying again through a separate standalone hard-wired Manual Safety Logic (MSL) Unit. This provides an independent and diversified implementation to prevent any mal-operation of the system and takes the system to the safe state during any fault conditions.

Index Terms— FHCS, MSL Unit, Interlock Implementation.

I. Introduction

The Fuel Handling Control System (FHCS) of Advanced Heavy Water Reactor (AHWR) is used for the refueling operation and control of Fueling Machine (FM), Fuel Transfer Machine (FTM) and other fuel handling equipments [1].

Considering the safety of fuel handling equipments which are operated remotely, the interlocks [2] have been designed to prevent any mal-operation and damage to its components. Interlocks are the instrumented functions that protect the machine and its components against failures of the plant system components, sensors, electronics etc. or incorrectly initiated operation. Manual Safety Logic (MSL) Unit implements the interlocks for safe operation of Fuelling Machines in Reactor using Field Programmable Gate Array (FPGA). FPGA based design approach was chosen because of its advantages such as all the digital integrated circuits (ICs) will be implemented on one single FPGA, fast processing time, Long-term maintenance and its reliability [3, 4].

II. Fuel Handling Control System

Fuel Handling Control (FHC) system is used for controlling Fueling Machine (FM), Fuel Transfer Machine (FTM), and other fuel handling equipments [1]. FHCS deploys two sets of Control Computers for FM and FTM respectively. Control Computers controls all FM and FTM related refueling and fuel transfer operations.

The control computer receives inputs from field devices, carries out control algorithm (to check safety interlocks) and processes them in conjunction with commands entered by the operator & drives output to operate field devices.

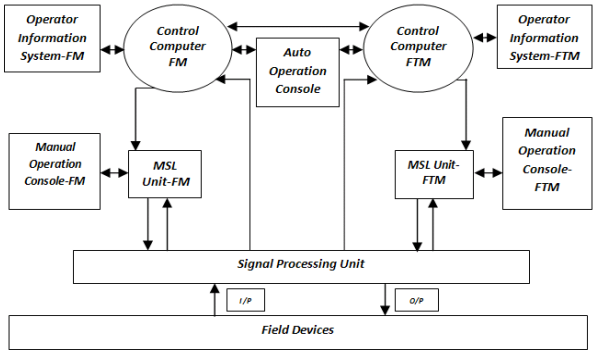

Figure 1: Block Diagram of Fuel Handling Control System

III. Manual Safety Logic Unit

Interlocks are provided to ensure safety during operation. Interlocks are soft coded in Control Computer and Hardwired in MSL Unit. If there is any deviation from the normal /safe operation due to any cause, it would be detected and compensated by initiating corrective actions. Interlocks provided for the safe operation of various actuator/ drives/ equipment/ process systems are derived by logical combination of various field signals [5].

The commands issued by control computers even after checking soft coded interlocks in auto-mode or by the operator from the main control panel / local panels in manual mode are fed to

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Manual Safety Logic Unit to check for the hard-wired interlocks.

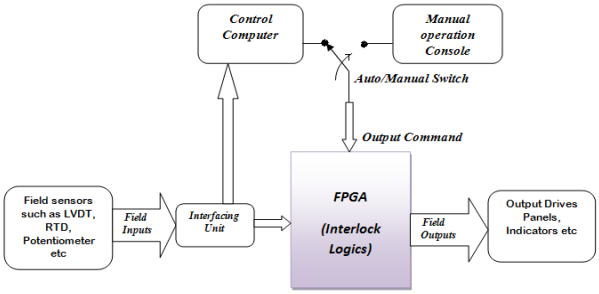

Figure 2: Manual Safety Logic Unit [5]

The interlocks will be implemented using programmable logic devices such as Field Programmable Gate Arrays (FPGA). Although FPGAs have fixed logic cells but they can hold a very large amount of logic implementation in a single IC, thereby reducing space requirement. In FPGA the required functions and the interconnections between them are determined by the user. The amount of wiring required is meager. The most important feature of FPGAs is it has the ability of parallel processing. VHDL being a strongly typed programming language was preferred for the design of MSL Unit. Since strongly typed programming languages permit a high level of checking by the compiler and reduce the probability of faults in the design. Various tools and techniques are presently available for independent verification and validation of the implementation of the requirements.

IV. DESIGN OF MSL

Electronic devices such as signal conditioners, Isolation relays, signal multipliers, signal comparators are used for processing input signals to drive outputs. The inputs can be either in the form of digital or analog signals. Field inputs are sensing devices such as LVDT & Potentiometer (for analog signals), Reed/ Limit switches and push buttons (for digital signals). Field outputs are drive outputs and panel outputs are indicators.

i. *Digital Input Module (DIM):* It is used for interfacing contact inputs such as push buttons, limit switches, proximity switches, pressure switches, level switches, glass switches etc to MSL cards. This module consists of signal conditioning, input low pass filter, Schmitt trigger and voltage clamping or clipping.

ii. *Digital Output Module (DOM):* It is used for interfacing output of MSL card to solenoid drivers or relays etc. It consists of filter to eliminate effect of voltage transients and electrical noise to protect from overload and short circuit.

iii. *Analog Isolation Module (AIM):* This module isolates the field analog signals and reduces noise pickup and eliminates ground loops in the system.

iv. *Differential Amplifiers (DF):* It amplifies the absolute value of difference between two analog field signals.

v. *Comparator Unit (CU):* It compares analog field signal with reference signal from the CSPU. Based on the comparison, CU generates digital signals that are used in MSL card.

vi. *Comparator Set Point Unit (CSPU):* It consists of independent potentiometers for generating the set point.

vii. *Solenoid Driver:* It is required for remotely energizing solenoids/relays.

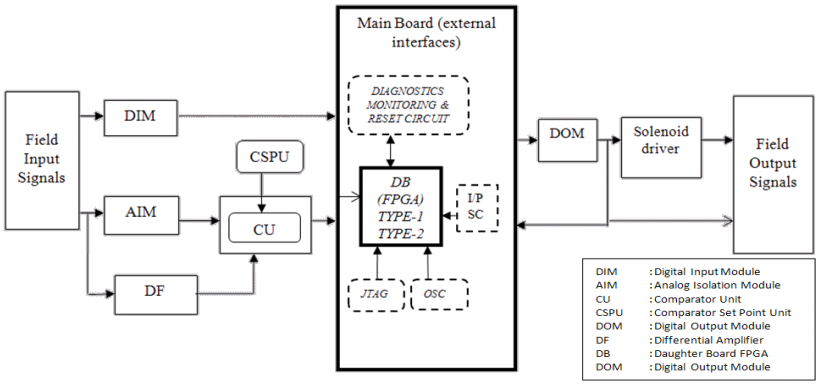

Figure 3: Design of MSL

The FPGA takes the data from the input modules and process the inputs based on interlock logics and results are passed through the drives. During auto-operation, the output of Control Computers is driven

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through MSL Unit to verify again using hardwired interlocks. Independent and diversified double checking of interlocks ensures the safe operation of fuel handling equipments. During manual mode of operation, 2/2 logic are used in critical areas to ensure safety so that failure of a single component will not lead to issue of wrong operate commands to the field.

V. Experimental Results

Fuel Handling System (FHS) consist of Fueling Machine components and Fuel Transfer Machine components for refueling and transferring of fuel respectively. As a representation Interlock implementation of FM component i.e. RAM assembly is described. RAM assembly can be operated in advance movement or retract movement. After the data is acquired based on the input values, output signals will drive only after satisfying the interlocks (algorithm). i_clk, i_rstb, data, data_out are the signals used for data acquiring. Data acquire at data_out signal depends on i_clk and i_rstb.

Based on the acquired values at data_out signal, the conditions *y1*, *y2* and *y3* manipulate its signals. AO20 is for advance operation and AO21 for retract operation. AO20 and AO21 will drive actuators after satisfying all necessary conditions. RAM assembly can be operated in either of both cases. RTL view and the simulated results are as shown in Fig 4 and 5.

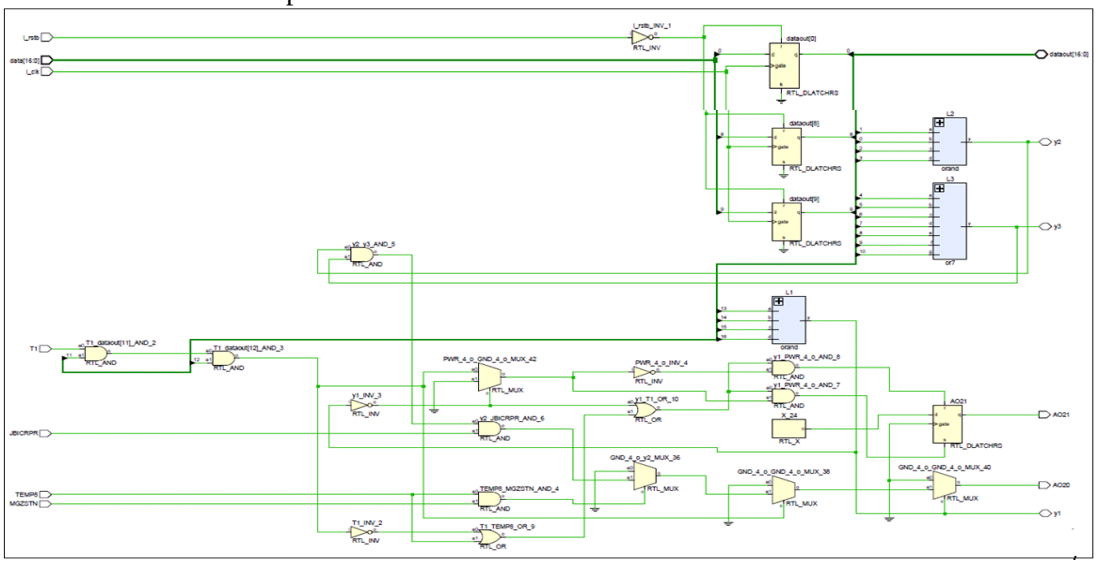

Figure 4: RTL view of RAM B Interlock

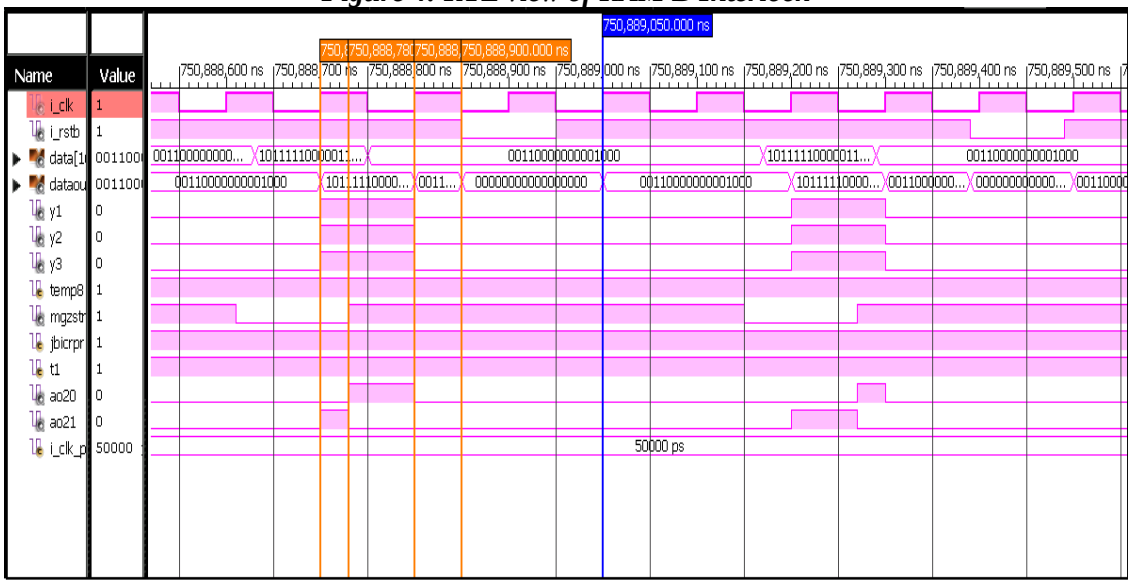

Figure 5: Simulated Result of RAM Assembly Interlock

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VI. Conclusion and Future Scope

MSL unit implements hard-wired interlocks using FPGA. Interlocks prevent mal-operation of the system. FHCS operates in auto mode or in manual mode. In this paper hardwired interlock implementation is discussed. The simulated results and RTL view for RAM assembly interlock are as shown in figure 4 & 5. Basically interlocks are the instrumented functions need to be verified before any operation is to be executed by Fuel Handling Components. These functions can be determined by users after a detailed study of equipments.

In critical areas 2/2 logic are used to ensure safety so that failure of a single component will not lead to issue of wrong operate commands to the field.

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