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A New Cascaded 2-Level Inverter based MultilevelSTATCOM for High Power Applications

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Abstract—A simple and reliableSTATCOM(static compensator) scheme for static varcompensation and power quality improvement are discussed in this paper. The topologies consist coupleoftwo level voltage source inverter. LV side of three phase coupling transformer is connected to cascaded inverter. DC-link voltages of two inverters are maintained at a specific ratio and operated as four-level inverter.For cascaded inverters, DC link voltage balancing of inverter are major task. The proposed system are investigated under MATLAB/SIMULINK and the results are verified for balanced and unbalanced conditions.

I. INTRODUCTION

Generation and transmission of power is complex process, it requires working of many components to produce maximum output. In which, the main component is reactive power in the system. To deliver the required active power through transmission lines, voltage is needed to be maintained. Reactive power is required for operation of loads such as motor loads and other inductive loads [1],[2]. At present, a widerange of very flexible controllers, which capitalize on newly available power electronics components, areemerging for custom power applications. Among these, STATCOM is popularly accepted as a reliable reactivepower controller replacing conventional var compensators, such as the thyristor-switched capacitor (TSC) andthyristor-controlled reactor (TCR). This device provides reactive power compensation, active power oscillationdamping, flicker attenuation, voltage regulation, etc.[3][4]and[5].The VSC connected in shunt with the ac system provides a multifunctional topology which can be used for up tothree quite distinct purposes [6][7].

Generally, in high-power applications, Var compensation is achieved using multilevel inverters [8]. These inverters consist of a large number of dc sources which are usually realized by capacitors. Hence, the converters draw a small amount of active power to maintain dc voltage of capacitors and to compensate the losses in the converter. However, due to mismatch in conduction and switching losses of the switching devices, the capacitors voltages are unbalanced. Balancing these voltages is a major research challenge in multilevel inverters. Various control schemes using different topologies are reported in [9]–[10].

Static Var compensation by cascading conventional multi-level/two level inverters is an attractive solution for highpower applications. The topology consists of standard multilevel/two- level inverters connected in cascade through open-end windings of a three-phase transformer. Such topologies are popular in high-power drives [11]. One of the advantages of this topology is that by maintaining asymmetric voltages at the dc links of the inverters, the number of levels in the output voltage waveform can be increased. This improves PQ [12]. Therefore, overall control is simple compared to conventional multilevel inverters. Various var compensation schemes based on this topology are reported in[13]–[14]. In[12], a three-level inverter and two level inverter are connected on either side of the transformer lowvoltage winding. The dc-link voltages are maintained by separate converters. In [15], three-level operation is obtained by using standard two-level inverters. The dc-link voltage balance between the inverters is affected by the reactive power supplied to the grid.

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In this paper, a static var compensation scheme is proposed for a cascaded two-level inverter-based multilevel inverter. The topology uses standard two-level inverters to achieve multilevel operation. The dc-link voltages of the inverters are regulated at asymmetrical levels to obtain four-level operation. To verify the efficacy of the proposed control strategy, the simulation study is carried out for balanced and unbalanced supply-voltage conditions. The dc-link voltages of two inverters collapse for certain operating conditions when there is a sudden change in reference current. In order to investigate the behavior of the converter, the complete dynamic model of the system is developed from the equivalent circuit.

This paper is organized as follows: The proposed control scheme is presented in Section II. Stability analysis of the converter is discussed in Section III. Simulation results are presented in Sections IV.

II. SINGLE TWO-LEVEL INVERTER-BASED STATCOM

Fig. 1 shows the power systemmodel considered in this paper [3]. Fig. 2 shows the circuit topology of the single two-level inverter-based STATCOM. The inverter is connected on the low-voltage (LV) side of the transformer and the high-voltage (HV) side is connected to the grid.

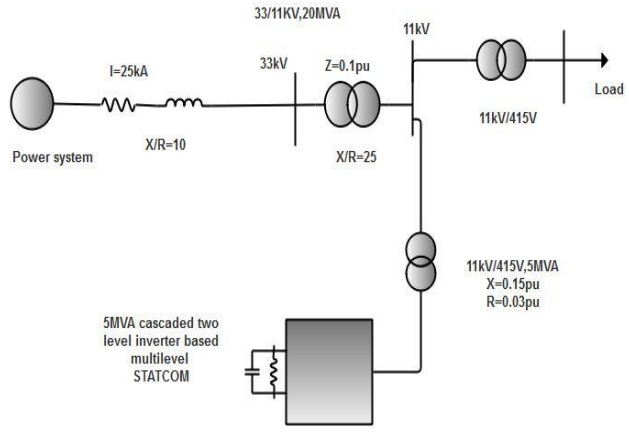

Fig. 1. Power system and the STATCOM model

A three phase inverters are used to provide industrial applications by adjustable frequency power. Three phase inverters are more common than single phase inverters. DC supply for three phase inverters is taken from a battery or usually from a rectifier. A six steps bridge is used for three phase inverter by using six switches, two switches for each phase. Each step is defined as a change in the time operation for each transistor to the next transistor in proper sequence. For one cycle 360°, each step would be of 60° interval for a six step inverter. . Large capacitors are connected at the input terminal to make the DC input constant and also suppress the harmonics fed back to the source.

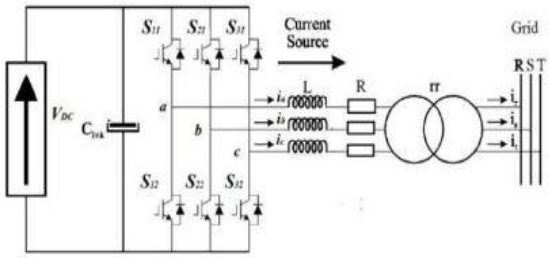

Fig. 2.Two-level inverter based STATCOM circuit topology

III. CASCADED TWO-LEVEL INVERTER-BASED MULTILEVEL STATCOM

Fig. 3 shows the circuit topology of the cascaded two-level inverter-based multilevel STATCOM using standard two-level inverters. The inverters are connected on the low-voltage (LV) side of the transformer and the high-voltage (HV) side is connected to the grid. The dc-link voltages of the inverters are maintained constant and modulation indices are controlled to achieve the required objective. The proposed control scheme is derived from the ac side of the equivalent circuit which is shown in Fig. 4

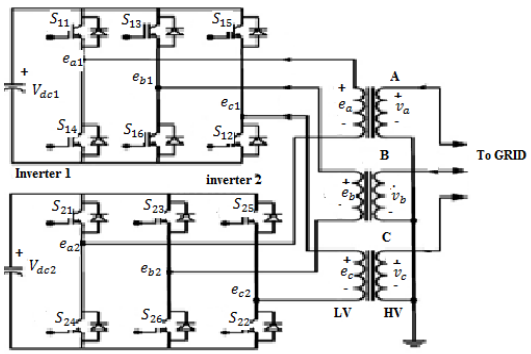

Fig. 3. Cascaded two-level inverter-based multilevel STATCOM

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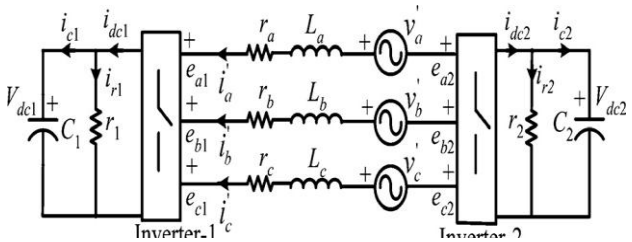

Fig. 4. Equivalent circuit of the cascaded two-level inverter-based multilevel STATCOM

From the Fig.4, the three phase RMS source voltages Va', $Vb'$and Vc' referred to the low-voltage side of the transformer. The leakage inductances of low-voltage side windings of the transformer are La, LbandLcrespectively. The transformer losses are represented in terms of resistances, which are ra, rbandrcrespectively. The output voltages of inverter1 and inverter2 are ea1,eb1, ec1and ea2, eb2, ec2. Finally leakage resistances of dc-link capacitors C1 and C2 are r1 and r2 respectively.

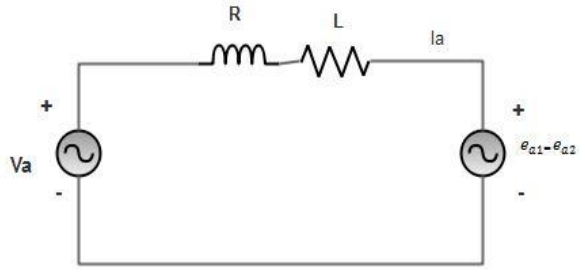

Fig. 4.Equivalent circuit of phase a

Equivalent circuit of phase „a" is shown in Fig.4. In the figure, the RMS source voltage is represented as va' , total loss in the system is represented as R, the transformer winding leakage inductance is represented as L, the voltage across primary side of the transformer of inverter1 and inverter2 is (ea1-ea2).

Applying KVL to the loop

$$-v_a' + R_a I_a' + L_a \frac{dI_a'}{dt} + (e_{a1}\text{-}e_{a2}) = 0 \quad (1)$$

Similarly for phase b and c,

$$-v_b' + R_b I_b' + L_b \frac{dI_b'}{dt} + (e_{b1}\text{-}e_{b2}) = 0 \quad (2)$$

$$-v_b' + R_c I_c' + L_c \frac{dI_c'}{dt} + (e_{c1}\text{-}e_{c2}) = 0 \quad (3)$$

By assuming resistances Ra = Rb= Rc = R and inductances

La = Lb = Lc = L, the above can be rewritten as,

$$\begin{bmatrix} \frac{di_a'}{dt} \\ \frac{di_b'}{dt} \\ \frac{di_c'}{dt} \end{bmatrix} = \begin{bmatrix} \frac{-r}{L} & 0 & 0 \\ 0 & \frac{-r}{L} & 0 \\ 0 & 0 & \frac{-r}{L} \end{bmatrix} \begin{bmatrix} i_a' \\ i_b' \\ i_c' \end{bmatrix} + \begin{bmatrix} \frac{1}{L} \end{bmatrix} \begin{bmatrix} v_a' - (e_{a1} - e_{a2}) \\ v_b' - (e_{b1} - e_{b2}) \\ v_c' - (e_{c1} - e_{c2}) \end{bmatrix} \quad (4)$$

The equation (4) is known as mathematical model in the stationary reference form of cascaded two-level inverter based STATCOM. To control both the active and reactive currents independently, above stationary reference frame equations can be converted into rotating reference frame equations. The source voltage of q-component is set to be zero so that the source voltage of d-component can be align with the synchronously rotating reference frame.

The dynamic model in the synchronously rotating reference frame is give as

$$\begin{bmatrix} \frac{di_d'}{dt} \\ \frac{di_q'}{dt} \end{bmatrix} = \begin{bmatrix} \frac{-r}{L} & \omega \\ -\omega & \frac{-r}{L} \end{bmatrix} \begin{bmatrix} i_d' \\ i_q' \end{bmatrix} + \begin{bmatrix} \frac{1}{L} \end{bmatrix} \begin{bmatrix} v_d' - (e_{d1} - e_{d2}) \\ -(e_{q1} - e_{q2}) \end{bmatrix} \quad (5)$$

Herev_d'represents the direct axis voltage component of ac source andi_d' , i_d'represents d-axis and q-axis current components of cascaded two-level inverter.

A. Control Strategy

Fig. 5 shows the block diagram of controller of the complete system. The d-axis and q-axis voltages can be controlled as,

$$e_d^* = -x_1 + \omega L i_q' + v_d' \quad (6)$$

$$e_q^* = -x_2 - \omega L i_d' + v_d' \quad (7)$$

Where $e_d^*$and $e_q^*$are d-axis and q- axis reference voltage components of the cascaded inverter. The parameters $x_1$and $x_2$are known as control parameters and they are controlled as,

$$x_1 = k_{p1} + \frac{k_{i1}}{s}(i_d^* - i_d') \quad (8)$$

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$$x_2 = k_{p2} + \frac{k_{i2}}{s}(i_q^* - i_q') \quad (9)$$

Where i_d^* is the direct (d)-axis reference current and is given by

$$i_d^* = (k_{p3} + \frac{k_{i3}}{s})\,[(V_{dc1}^* + V_{dc2}^*) - (V_{dc1} + V_{dc2})] \quad (10)$$

The reference voltages of dc-link capacitors of inverter 1 and inverter2 are V_{dc1}^* and V_{dc2}^*. The reference reactive current component is the q-axis component(i_q^*),can be obtained either from load,or from voltage regulation loop.

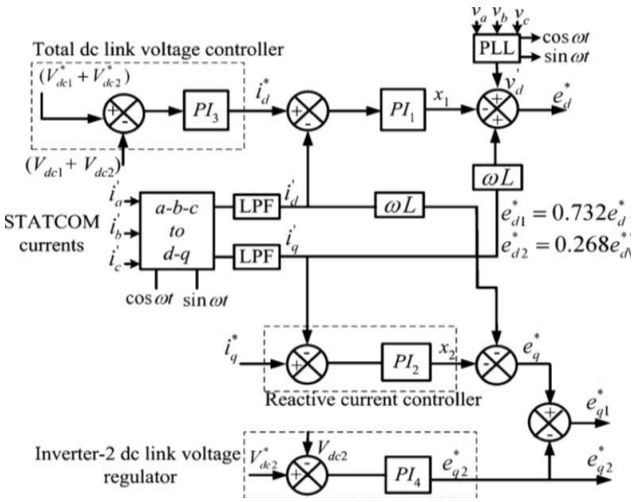

Fig. 5. Control block diagram.

From the control diagram it is clear that, three phase voltages V_a, V_b, V_c are given to phase-locked loop (PLL) and unit signals cosωt and sin ωt are generated. Phase locked loop (PLL) is used to generate output signal to match the phase of input signal. These unit signals are transforms the converter currents i_a', i_b', i_c into synchronously rotating reference frame currents. So reactive and active current components can be easily controlled. Switching frequency ripples can be eliminated by using low-pass filters (LPF). The reference voltages to the converter are (e_d^*, e_q^*) are generated from controller using $(V_{dc1}^* + V_{dc2}^*)$ and reference reactive current. The inverter supplies desired reactive current component and draws active component of current.Which can be further used to regulate total dc-link voltage of $(V_{dc1}^* + V_{dc2}^*)$ the inverter.

B. DC-Link Balance Controller

The total dc-link balance controller is used to provide magnitude and phase of resultant voltage supplied by the cascaded inverter. The active power sharing between the inverter and grid is depends on angle δ. From the figure, the reference voltage components of q-axis of the two inverters e_{q1}^*, e_{q2}^* is obtained as

$$e_{q1}^* = e_q^* - e_{q2}^* \quad (11)$$

$$e_{q2}^* = (k_{p4} + \frac{k_{i4}}{s}) + (V_{dc2}^* - V_{dc2}) \quad (12)$$

Where e_{q1}^* controls the inverter1 dc-link voltage, e_{q2}^* controls the inverter2 dc-link voltage. The dc-link voltage of inverter 2 is controlled at 0.366 times dc-link voltage of inverter 1, so four level operation is obtained and output voltage harmonic spectrum is improved. The inverter1 dc-link voltage and inverter2 dc-link voltage is expressed in terms of total dc-link (V_{dc}) voltage.

$$V_{dc1} = 0.732 V_{dc} \quad (13)$$

$$V_{dc2} = 0.268 V_{dc} \quad (14)$$

The power transfer to inverter1 is indirectly controlled and for inverter2, power transfer is directly controlled. Therefore inverter2 attain its reference value quickly when compared to inverter1. The control circuit uses the sinusoidal pulse width modulation (SPWM) technique to generate gate signals from the obtained reference voltages.

C. Unbalanced Conditions

Due to fault or unbalance in the system, negative-sequence voltage appears in the supply voltage and results in double supply frequency component in the dc-link voltage of the inverter. This double frequency component injects the third harmonic component in the ac side. Due to negative-sequence voltage, large negative-sequence current flows through the inverter which may cause the STATCOM to trip. Therefore, during unbalance, the inverter voltages are controlled in such a way that either negative-sequence current flowing into the inverter is eliminated or reduces the unbalance in the grid voltage. In the latter case, STATCOM needs to supply large currents since the interfacing impedance is small. This may lead to trip- ping of the converter.

IV. SIMULATION RESULTS

The system configuration shown in Fig. 1 is considered for simulation. The simulation study is

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carried out usingMATLAB/ SIMULINK. The system parameters are given in Table I.

TABLE I
SIMULATION SYSTEM PARAMETERS

Rated power	5 MVA
Transformer voltage rating	11kv/400
AC supply frequency	50 Hz
Inverter-1 dc link voltage	659 V
Inverter-2 dc link voltage	241 V
Transformer leakage reactance	15%
Transformer resistance	3%
DC link capacitance	50mF
Switching frequency	1200Hz

TABLE II
SIMULATION RESULT OF BASE SYSTEM

Sl.no	Real power	Reactive power
1	8.12MW	5.85MVar

A. Simulation and analysis of complete system with cascaded two level STATCOM

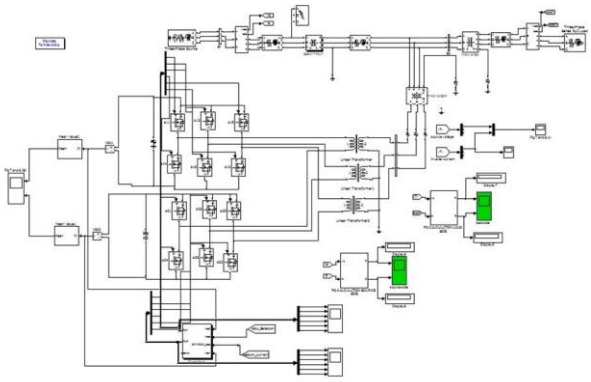

Fig. 6.Simulink model of system with cascadedtwo level STATCOM

a. *Reactive Power Control*

In this case, reactive power is directly injected into the gridby setting the reference reactive current component at a particular value. Initially,i_q^* is set at 0.5p.u. At t=2.0 s, i_q^*ischanged to 0.5p.u. Fig.13 shows the dc-linkvoltages of two inverters. From the figure, it can be seen that thedc-link voltages of the inverters are regulated at their respective reference valueswhen the STATCOMmode is changed from capacitiveto inductive. Moreover, the dc-link voltage of inverter 2 attains its reference value faster compared to that of inverter 1.

b. *Load Compensation*

In this case, the STATCOM compensates the reactive power of the load. Initially, STATCOM is supplying a current of 0.5p.u. At t= 2.0 s, the load current is increased so that STATCOM supplies its rated current of 1 p.u.Fig.14shows the dc-link voltages of two inverters. The dc-link voltages are maintained at their respective reference values when the operating conditions are changed.

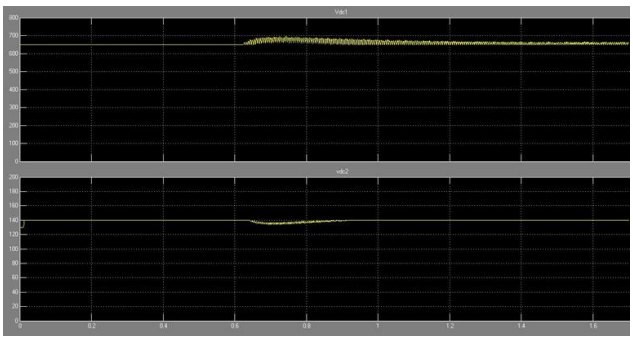

Fig.7.Ractive power compensation-DC link voltages of two inverters

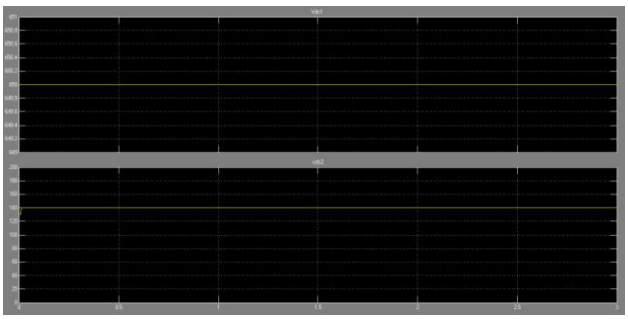

Fig. 8.Load compensation-DC link voltages of two inverters

c. *Operation During the Fault Condition*

In this case, a single-phase-to-ground fault is created at t= 1.2 s, on the phase of the HV side of the 33/11-kVtransformer. The fault is cleared after 200 ms. Fig. 14(a) shows voltages across the LV side of the 33/11-kV transformer. Fig. 14(b) shows the - axes components of negative-sequence current of the converter. These currents are regulated at zero during the fault condition.

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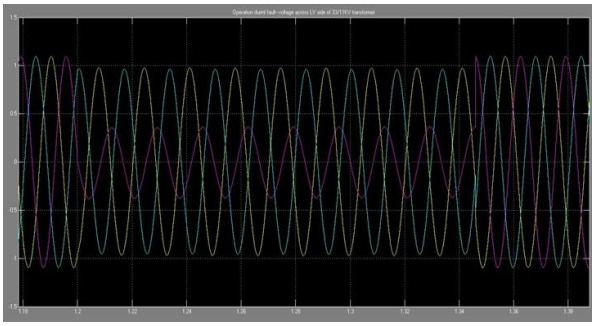
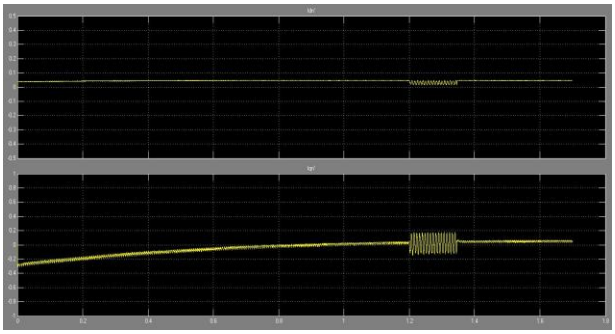


Fig. 9(a).Operation during fault. (a) Grid voltages on the LV side of the transformer.



9(a).(b).Operation during fault -d-axis negative-sequence current component and q-axis negative-sequence current component

TABLE IV

SIMULATION RESULT OF SYSTEM CASCADED TWO LEVEL STATCOM

Sl.no	Real power	Reactive power
1	9.25MW	0.885MW

V.CONCLUSION

In cascaded inverter based STATCOM the DC-link voltage balance is the major issue.This paper presents cascaded H-bridge inverter based multi-level static compensator (STATCOM).The main objective is to compensate the reactive power with the improved power quality. Sinusoidal pulse width modulation have better control on output voltage magnitude, they accounts for harmonics in the output voltage.In this paper, a simple var compensating scheme is proposed for a cascaded two-level inverter- based multilevel inverter. The scheme ensures regulation of dc-link voltages of inverters at asymmetrical levels and reactive power compensation. The performance of the scheme is validated by simulation.

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