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Design, Implementation and Analysis of a High Speed Multiplier for Low Power Application

Vinutha P[1], Praveen Kumar Y G[2],Dr. M Z Kurian[3]
[1]Student, M. Tech (VLSI and Embedded Systems), SSIT, Tumakuru
[2]Asst.Prof, Dept. of ECE,SSIT, Tumakuru
[3]HOD, Dept.of ECE, SSIT, Tumakuru

Abstract-Multiplier design is always a challenging task; how many ever novel designs are proposed, the user needs demands much more efficient one. Vedic mathematics is world renowned for its algorithms that yield quicker results, be it for mental calculations or hardware design. Power dissipation is drastically reduced by the use of Reversible logic. The reversible UrdhvaTiryakbhayam Vedic multiplier is one such multiplier which is effective both in terms of speed and power. This multiplier is designed and implemented using reversible logic Feynman Gate, Peres Gate and HNG gate. Feynman and Peres gates are used to implement the basic two bit multipliers and HNG gate is used as full adder for summation of the partial product generated by two bit multipliers in four bit multiplierThe main aim and purpose of this paper is to improve the speed and to reduce the power dissipation of the processor by using efficient Vedic multiplier. Vedic multiplier using reversible logic for high speed and less delay has been implemented using the cadence tool.

Key Words: Low power CMOS design, Reversible Logic, quantum computing, Vedic Multiplier, Urdhava Sutra.

1. INTRODUCTION

Vedic Mathematics is one of the most ancient methodologies used by the Aryans in order to perform mathematical calculation . This consists of algorithms that can boil down large arithmetic operations to simple mind calculations. The above said advantage stems from the fact that Vedic mathematics approach is totally different and considered very close to the way a human mind works.

The efforts put by Jagadguru Swami Sri Bharati Krishna Tirthaji Maharaja to introduce Vedic Mathematics to the commoners as well as streamline Vedic Algorithms into 16 categories or Sutras needs to be acknowledged and appreciated. The UrdhvaTiryakbhayam is one such multiplication algorithm which is well known for its efficiency in reducing the calculations involved.

Multiplication is the process of adding a number of partial products. Multiplication algorithms differ in terms of partial product generation and partial product addition to produce the final result. Higher throughput arithmetic operations are important to achieve the desired performance in many real time signal and image processing applications. With time, many researchers have tried to design multipliers which offer either of the following- low power consumption, high speed, regularity of layout. However, the two design criteria are often in conflict one is the fast multiplication feature derived from Vedic algorithm, Nikhilam sutra and another is the reduced heat dissipation by the virtue of implementing the circuit using reversible logic gates. The conventional mathematical algorithms can be simplified and even optimized by the use of Vedic mathematics. By using this technique the speed of the processor can be improved to perform fast arithmetic operations.

Reversible logic is a promising computing design paradigm which presents a method for constructing computers that produce less heat. Reversible computing emerged as a result of the application of quantum mechanics principles towards the development of a universal computing machine. Specifically, the fundamentals of

reversible computing are based on the relationship between entropy, heat transfer between molecules in a system, the probability of a quantum particle occupying a particular state at any given time, and the quantum electrodynamics between electrons when they are in dose proximity, the basic principle of reversible computing is that a bi-jective device with an identical number of input and output lines

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will produce a computing environment where the electrodynamics of the system allow for prediction of all future states based on known past states, and the system reaches every possible state, resulting in no heat dissipation A reversible logic gate is an N-input, N-output logic device that provides one to one mapping between the input and the output. It not only helps us to determine the outputs from the inputs but also helps us to uniquely recover the inputs from the outputs. Garbage outputs are those outputs which do not contribute to the reversible logic realization of the design. Quantum cost refers to the cost of the circuit in terms of the cost of a primitive gate. Gate count is the number of reversible gates used to realize the function. Gate level refers to the number of levels which are required to realize the given logic functions.

2. LITERATURE SURVEY

Landauer.R.[1],in computing process, a research has been done on irreversibility and heat generation and he demonstrated that a high complex circuit and system which are constructed due to a onbit of information loss using irreversibility hardware results in energy dissipation. According to the previous researches, the loss of one bit information dissipates at least KTln2 joules of energy, where K is the Boltzmann's constant and T is the absolute temperature at which the operation is performed. The heat generated due to the loss of one bit of information is very small at room temperature but when the number of bits is more in the high speed computational work, the generated by them will be very large.

Bennett C.H.[2], in 1973 the concept of reversible logic came into existence. He discovered that power dissipation in any circuit can be minimized by using the reversible logic method.

Ktln2 joules of energy dissipation can be reduced using a reversible logic based circuit. Bennett showed that an irreversibly performed machine can also be made reversible with the same efficiency. Large amount of temperature storage needed for the history is one of the disadvantage of the reversible machine.

Ch. Harish Kumar.[3],in this paper author has Proposed the two sutra's which are used for the multiplication i.eUrdhvaTriyakbhyam and Nikhilam Sutra are compared. The system implementation of basic 2X2 multiplier, 8X8 multiplier for UrdhavaTiryakbhyam and Nikhilam Sutra are discussed and compared. The results of 8X8, 16X16 and 32X32 multipliers are compared. To show the results between Vedic and conventional multipliers array multiplier has been taken. In terms of power, delay and area the results are compared. Vedic multipliers are to be the best compared to conventional ones as know that from the earlier. Compared to Nikhilam Sutra architecture UrdhvaTriyakbhyam is efficient on.

Shri Prakash Dwivedi. [4], the possibility of applying the Nikhilam sutra of Vedic mathematics is for the number which is near to the base. The advantage this sutra is that it converts a large-digit multiplication to respective small digit multiplication. When both multiplicand and multiplier are near to some base (radix) power Nikhilam method is particularly efficient.

3. SYSTEM DESIGN

In this section, detailed block diagram of proposed Vedic multiplier is explained.

3.1 Peres Gate

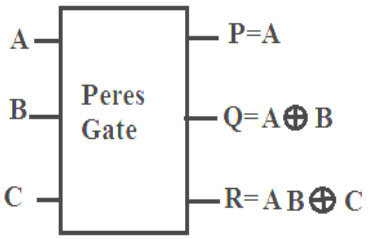

Figure 3.1: Peres Gate

Figure 3.1 shows a 3*3 Peres gate. The input vector is I(A, B, C) and the output vector is O (P, Q, R). The output is defined by P = A, Q= A xor Band R=AB xor C. Quantum cost of a Peres gate is 4. This gate is used in implementing 2 bit Vedic multiplier.

3.2 Feyman Gate

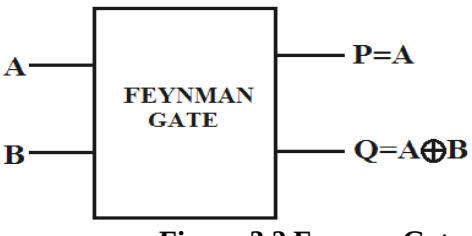

Figure 3.2 Feyman Gate

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Feynman gate is a 2*2 one through reversible gate as shown in Figure 3.2. The input vector is I(A, B) and the output vector is O(P, Q). Quantum cost of a Feynman gate is 1. This gate is used in implementing 2 bit Vedic multiplier.

3.3HNG Gate

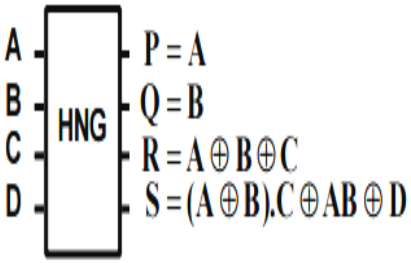

Figure 3.3: HNG Gate

Figure 3.3 shows the 4x4 HNG gate. A single HNG gate can serve as a one bit full adder. Quantum cost of this gate is six. This gate is used in implementing bit ripple carry adder.

3.4 Implementation of 2 bit Vedic multiplier

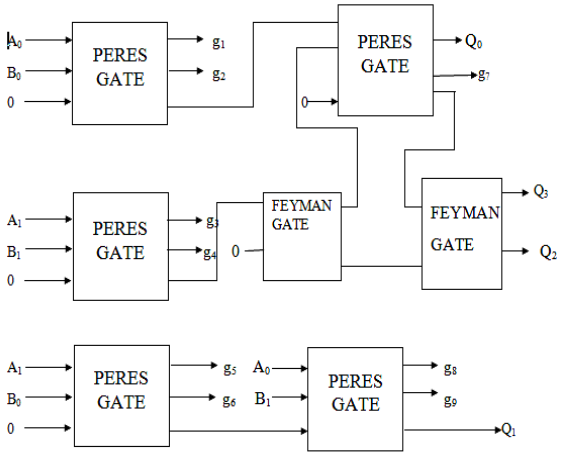

Figure 3.4 2 Bit Vedic Multiplier

Figure 3.4 shows a 2 bit Vedic multiplier using reversible gates which uses five Peres gates and two Feynman gate. This design has a total quantum cost of 22, number of garbage outputs are 9 and number of constant inputs 5. The gate count is 7. The overall performance of the multiplier is scaled up by optimizing each individual unit in terms of quantum cost, garbage outputs.

This 2 bit Vedic multiplier has been used to built 2 bit Vedic multiplier and for that a 4 bit ripple carry adder and four 2 bit Vedic multiplier is required.

3.5. Implementation of 4 bit ripple carry adder.

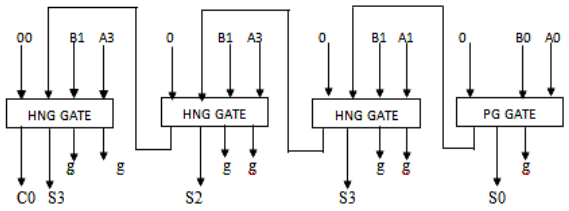

Figure 3.5: 4 Bit Ripple Carry Adder

Figure 3.5 shows the implementation of 4 bit ripple carry adder using HNG gates and peres gate. The number of HNG gates is 3 and peres gate is 1. For any ripple carry adder the input carry for the first full adder is zero, this implicitly means the first adder is a half adder. Thus a Peres gate can be efficiently replaces a HNG gate.

This cut down the quantum cost by two for any ripple carry adder and the garbage output by one. So the total quantum cost of the 4 bit multiplier is 22 and garbage output is 7. The Constant inputs and the gate count of 4 bit ripple adder is 4 and 4 respectively.

3.6 Proposed 4 bit Vedic Multiplier

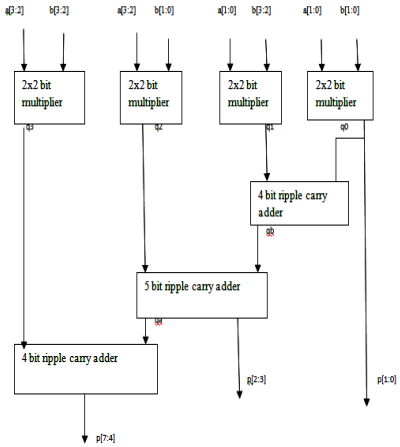

Figure 3.6: 4 bit Vedic multiplier

A 4 bit reversible Vedic multiplier is designed using 2 bit Vedic multiplier. The block diagram of 4 bit Vedic multiplier is shown in figure 3.6.

The block diagram consists of four 2 bit multiplier blocks each block has four bit inputs. Two bits from the multiplicand and other two bits from multiplier has been taken. Two zeros are concatenated with the upper two bits and given as input to the four bit ripple carry adder is obtained from the second 2 bit

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multiplier. The output of the second and third 2 bit Vedic multiplier block is given to the 4-bit ripple carry adder as an input which is designed using reversible HNG gate. The output of second ripple carry adder is given to the first 4-bit ripple carry adder. The sum 2-bits from first four bit ripple carry adder is taken as output of the 4x4 Vedic multiplier.

Another 2-bits sum output is given as an input to the third 4-bit ripple carry adder. The 4- bit output is taken from the fourth 2 bit Vedic multiplier and given as an input to the third 4-bit ripple carry adder designed using HNG gate.

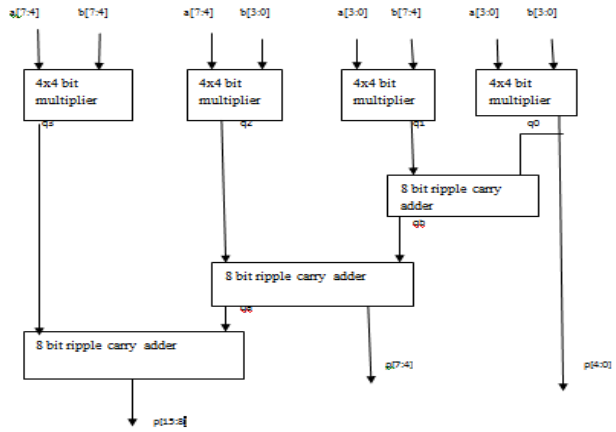
3.7 Proposed 8 Bit Vedic Multiplier

A 8 bit reversible Vedic multiplier is designed using 4 bit Vedic multiplier. The block diagram of 4 bit Vedic multiplier is shown in figure 3.7

The block diagram consists of four 4 bit multiplier blocks each block has four bit inputs. Two bits from the multiplicand and other two bits from multiplier has been taken. Two zeros are concatenated with the upper two bits and given as input to the four bit ripple carry adder is obtained from the second 2 bit multiplier.

The output of the second and third 2 bit Vedic multiplier block is given to the 4-bit ripple carry adder as an input which is designed using reversible HNG gate.. The sum 4-bits from first four bit ripple carry adder is taken as output of the 8x8 Vedic multiplier.

Another 2-bits sum output is given as an input to the third 8-bit ripple carry adder. The 4- bit output is taken from the fourth 2 bit Vedic multiplier and given as an input to the third 8-bit ripple carry adder designed using HNG gate.



4. RESULTS

Here Verilog HDL code for 2 bit Vedic multiplier is synthesized using cadence tool.. Figure 4.1, 4.2, and 4.3 shows the simulation result of 2 bit, 4 bit and 8 bit Vedic multiplier.

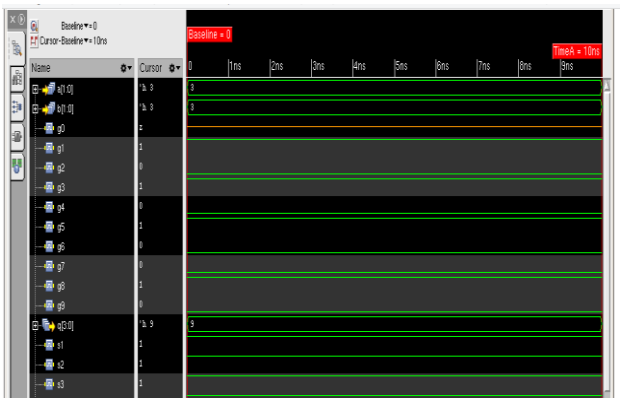


Figure 4.1: Simulation Result 2x2 Vedic Multiplier

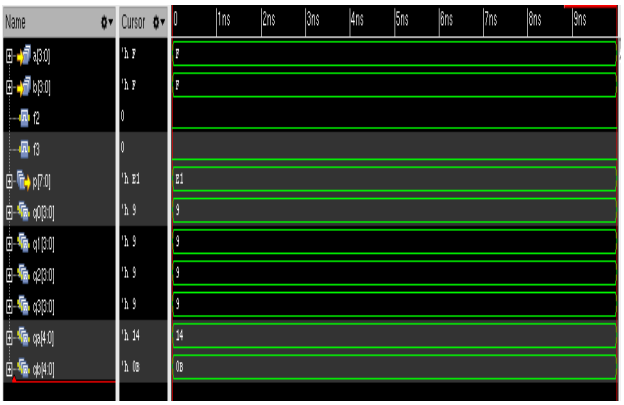


Figure 4.2: Simulation Result 4x4 Vedic Multiplier

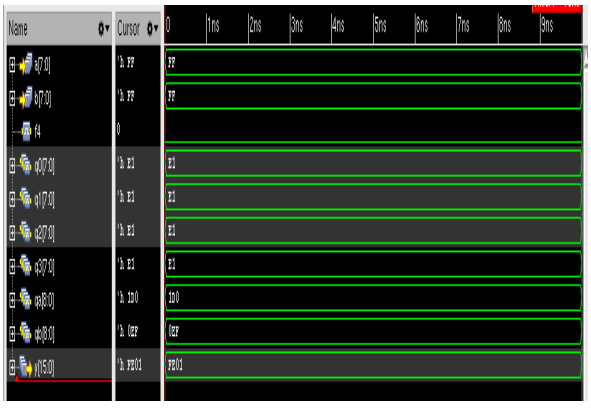


Figure 4.3: Simulation Result 8x8 Vedic Multiplier

4.4 Power Analysis

BITS	180nm	90nm
2	17.7829uw	3.931uW
4	28.485uW	12.695uw
8	738. 41uw	16.2uW

CONCLUSION

A 2 bit Vedic multiplier has been implemented using reversible gate. And using this 2 bit Vedic multiplier 4 bit and 8 bit Vedic multiplier is implemented using the cadence tool and power analysis has been done.

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