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Design and Analysis of CMOS based Low Power Carry Select Full Adder

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ABSTRACT: -Carry Select Adder (CSLA) is trusted to be one of the most speedster adders used in many data-processing processors to achieve faster arithmetic functions. From the structure of the CSLA, it is predicted that there is scope for reducing the area and power consumption in the CSLA. On the basis of this modification of 4-bit and 8-bit CSLA architecture, it has been developed and compared with the conventional CSLA architecture. The proposed design has reduced area and power as compared with the conventional CSLA with the minimum amount of delay. This work evaluates the performance of the proposed designs in terms of delay, area, power, and their products by hand with logical effort and through custom design and layout in 180nm. In this work we have presented systematic approach to construct full adders using conventional, 10T, transmission gates (TG) and binary to excess converter techniques (BEC). The results analysis concludes that the proposed CSLA (Carry Select Adders) structure is better than the normal regularly used CSLA (Carry Select Adders).

KEYWORDS: TG, low power design, BEC, 10T.

I. INTRODUCTION

Design low power VLSI system is significant due to the fast growing technology in communication. Enhancing the performance of full adders can significantly affect the performance of the whole system. To possess low power digital process, a low-powerful adder is preferred. Till now only 4-bit and 8- bit carry select adder has been designed. The results analysis concludes that the proposed CSLA (Carry Select Adders) structure is better than the regular CSLA (Carry Select Adders).

Many logic styles have been used in past for designing the full adder circuits .A full adder cell is implemented with 10 transistors with reduced power. The modified CSLA using BEC has reduced area and power consumption with slight increase in delay. CSA using transmission gate logic has shown better results than with CSA using logic gates in the aspect of power .The basic idea of the proposed architecture is that which replaces the 28 transistor to 10 transistors. The modified architecture reduces the area, delay and power. Large power consumption affects the circuits operation and reliability by increasing temperature of circuits.

CMOS process technology as reducing the nanometer technologies also reduces the power dissipation

II. REGULAR CONVENTIONAL FULL ADDER

A. Description

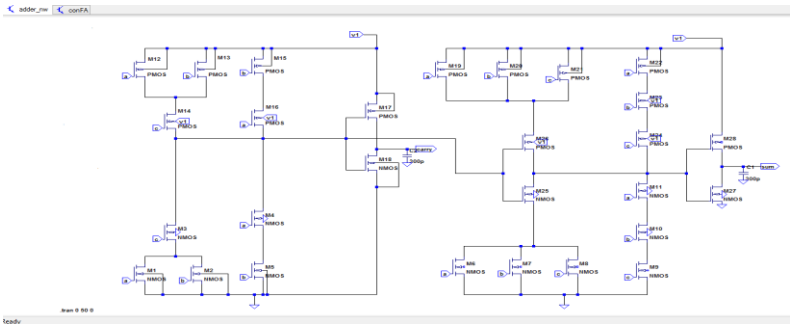

Fig 1:Schematic of Conventional Full Adder

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Complementary CMOS structure is invented utilizing consistent CMOS configuration of full adder which consists of PMOS pull-up and NMOS pull-down transistors shown in figure. Standard static CMOS full adder with pull up and pull-down networks used 28 transistors.

B. CSLA Using BEC

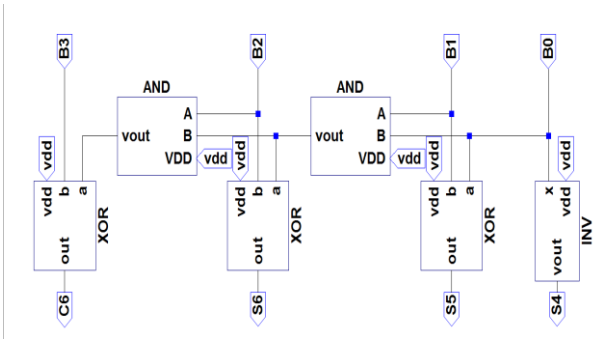

Fig 2: BEC

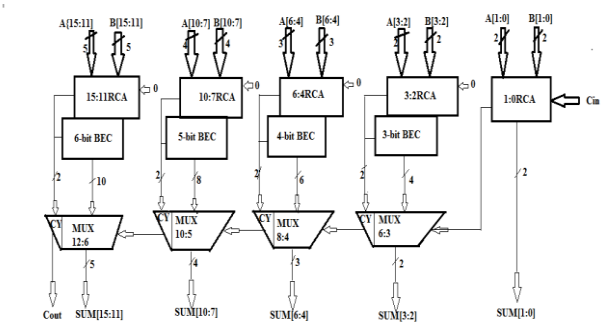

Fig 3: Full adder using BEC

The main idea of this work is to use BEC instead of the RCA with C_{in}=1 in order to reduce the area and power consumption of the regular CSLA. To change the 2-bit RCA, a 3-bit BEC and so on is required; the general function of the CSLA is obtained by using the3, 4-bit BEC together with the multiplexer. The main advantage of the BEC is the main silicon area reduction when the CSLA with large number of bits are designed.

III. PROPOSED METHOD

I. Description

Availability of complementary control signals, opting for the correct transistor types in contemplating the sum and carry modules become more flexible to abstain the occurrence of multiple threshold voltage loss. The degradation in output voltage swing can thus be minimized, which increases the efficiency of the design in low Vdd operations. Its capability of providing complementary ‘propagate’ control signals helps reduce the voltage degradation in the output generation stages.

II. Modified 10T architecture

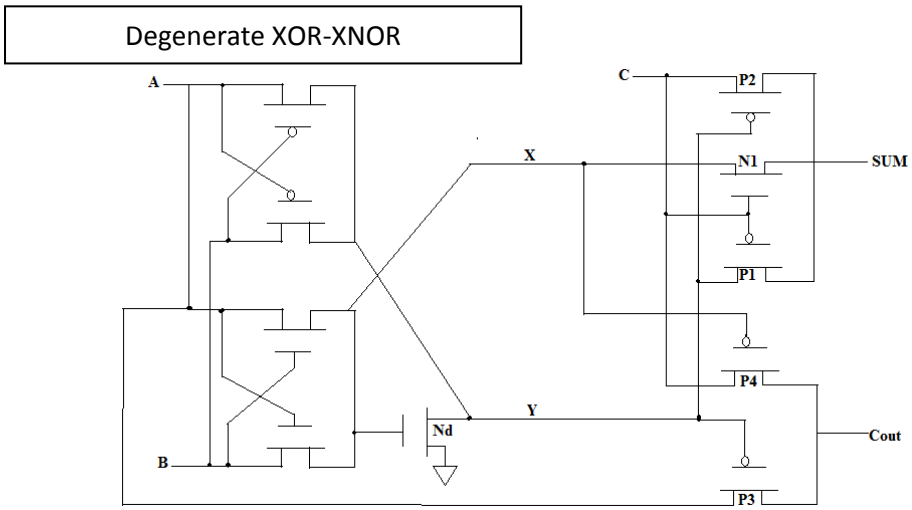

Fig 4: Full adder with 10T

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Table 1.The truth table of the degenerate XOR-XNOR

A	B	C	Y	X
0	0	0	0/0+	1-/0
		1	0	1-
0	1	—	1	0
1	0	—	1	0
1	1	—	0	1-

III. Modified Transmission Gate architecture

The transmission gate is additionally referred to as pass gates. Gate voltage applied to those gates is complementary of every other(C and Cbar). Transmission gates act as bidirectional switch between 2 nodes A and B controlled by signal C. Gate of NMOS is connected to C and circuit of PMOS is connected to C complemented (invert of c). Once management signal C is high, each semiconductor device area unit on and provides a low resistance path between A and B. On the opposite hand, once C is low each transistors area unit turned off and supply high resistance path between A and B.

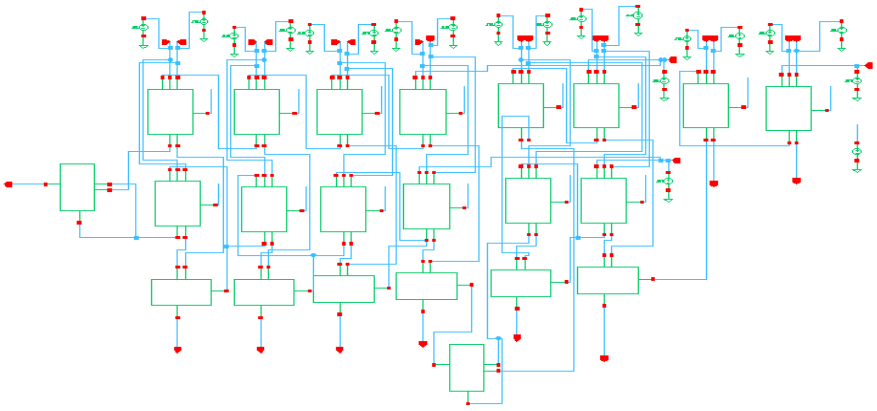

Fig 5: Full adder with Transmission Gate

IV. RESULT & SIMULATION

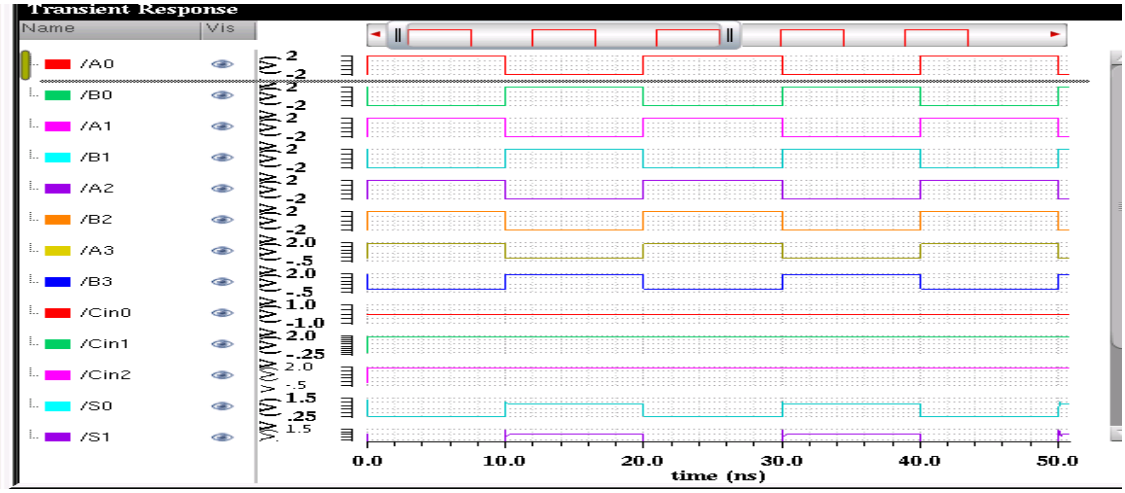

Fig: 6 Input Waveform

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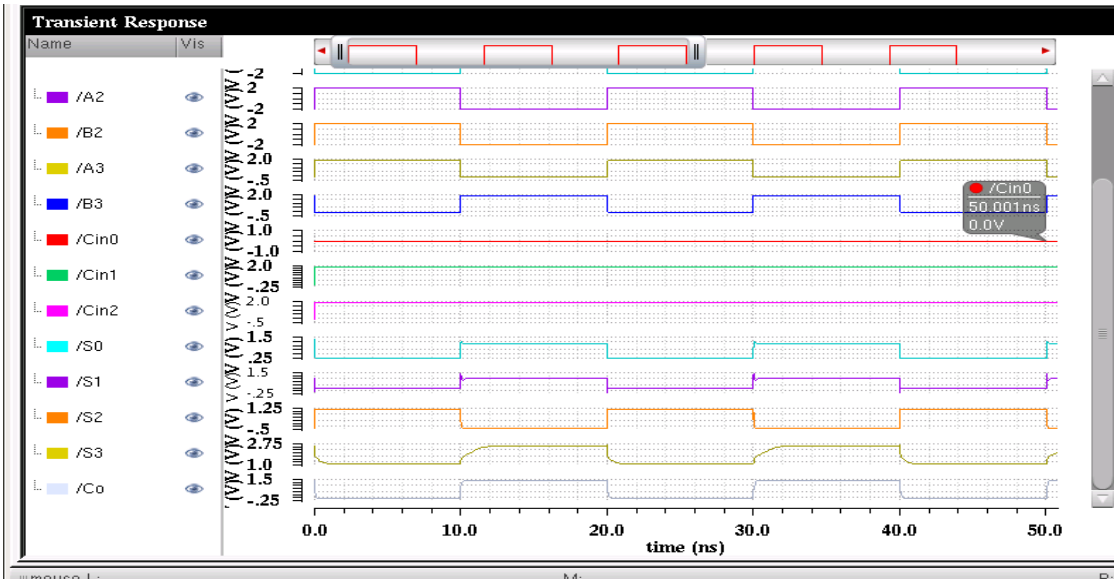

Fig: 7 Output Waveform

Table 2. Power Delay product comparison for 4 Bit CSA at 180nm

	Delay (pSec)	**Power (mWatt)**	**PDP (pJ)**
Conventional	28.5	178.4	5.084
10 T	11.44	148.6	1.699
Transmission Gate	17.1	104.1	1.780
Binary Excess 1 Converter	21.7	133.8	2.903

V. CONCLUSION

In this paper we've conferred systematic approach to construct full adder's victimization standard, 10T, and transmission gates, binary to excess convertor techniques. Based on our simulations, the new improved Transmission gate and 10T adder cell consume significantly less power within the order of small watts and has 46 percent higher speed and reduces 50 percent threshold loss drawback compared to the previous differing types of electronic transistor adders.

VI. REFERENCES

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