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Analysis on High Speed Convolution and Deconvolution Algorithm based on Ancient Indian Vedic Mathematics

[1]SD. Jaki Sharif, [2]Dr. T.Srinivas
[1](Research Scholar(25617081), Dept of ECE, Shri Jagadishprasad Jhabarmal Tibrewala Uinversity, Jhunjhunu, Rajasthan .&
Assistant professor, Dept. Electronic & Communication Engineering
Mother Theressa College of Engg & Tech. Peddapalli, , India
[2]professor, Dept. Electronic & Communication Engineering. Peddapalli, India

Abstract— *Convolution and Deconvolution is having wide area of application in Digital Signal Processing. Convolution helps to estimate the output of a system with arbitrary input, with knowledge of impulse response of the system. Linear systems characteristics are completely specified by the systems impulse response, as governed by the mathematics of convolution. And with the knowledge of impulse response and output of a system we recover the unknown input in Deconvolution operation. Convolution and deconvolution is central to many applications of Digital Signal Processing and Image Processing. In DSP the convolution and deconvolution with a long sequence is ubiquitous in many application areas and they consume much of time. Primary requirement of any application to work fast is that increase the speed of their basic building block. Multiplier and Divider is the heart of convolution and deconvolution respectively. It is most important but, slowest unit of the system and consumes much time in the system. Many methods are invented to improve the speed of the multiplier and divider, amongst all Vedic multiplier and divider is under focus because of faster working and low power consumption. In this project we have implemented the high speed convolution and deconvolution system using Vedic mathematics.*

Keywords—Convolution, Deconvolution, Vedic Mathematics , VHDL

I. INTRODUCTION

With the latest advancement of VLSI technology, digital signal processing plays a pivotal role in many areas of electrical and electronics engineering. High speed convolution and deconvolution is central to many applications of Digital Signal Processing and Image Processing, Convolution and Deconvolution having extreme importance in Digital signal processing. Convolution is having wide area of application like designing the digital filter, correlation etc. However it is quite difficult for the new candidate to perform convolution and deconvolution as convolution and deconvolution method is so lengthy and time consuming, beginners often struggle with convolution and deconvolution because the concept and computation requires a number of steps that are tedious and slow to perform. Many methods are proposed for performing convolution, one of a tough approach is a Graphical method, it is quite sophisticated and systematic but, it is very lengthy and time consuming. Therefore many of the researchers have been trying to improve performance parameters of convolution and deconvolution system using new algorithms and hardware. Complexity and excess time consumption are always the major concern of engineers which motivates them to focus on more advance and simpler techniques. Pierre and John have implemented a fast method for computing linear convolution. This method is similar to the multiplication of two decimal numbers and this similarity makes this method easy to learn and quick to compute. Also to compute deconvolution of two finite length sequences, a novel method is used. This method is similar to computing long-hand division and polynomial division. Principal components required for implementation of convolution calculation are adder and multiplier for partial multiplication. Therefore the partial multiplication and addition are bottleneck in deciding the overall speed of the convolution implementation technique. As adder is also an important block for the proposed method, so all

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required possible adders are studied. Adders which have the highest speed and occupy a comparatively less area, are selected for implementing convolution. Since the execution time in most DSP algorithms mainly depends upon the time required for multiplication, so there is a need of high speed multiplier. Now a days, time required in multiplication process is still the dominant factor in determining the instruction cycle time of a DSP chip. Traditionally shift and add algorithm is being used for designing. However this is not suitable for VLSI implementation and also from delay point of view. Some of the important algorithms proposed in literature for VLSI implementable fast multiplication are Booth multiplier, array multiplier and Wallace tree multiplier. Although these multiplication techniques have been effective over conventional ―shift and add‖ technique but their disadvantage of time consumption has not been completely removed. Vedic Mathematics provides unique solution for this problem. The Urdhva-Tiryagbhyam Sutra or vertically and crosswise algorithm for multiplication is discussed and then used to develop digital multiplier architecture. For division, different division algorithms are studied, by comparing drawbacks and advantages of each algorithm, Paravartya Algorithm based on Vedic mathematics is modified according to need and then used. Many engineering application areas use this Vedic Mathematics, especially in signal processing. It describes 16 sutras and sub-sutras which cover all the branches of mathematics such as arithmetic, algebra, geometry, trigonometry, statistics etc. Implementation of these algorithms in processors has found out to be advantageous in terms of reduction in power and area along with considerable increase in speed requirements. These Sutras are given in Vedas centuries ago. To be specific, these sutras are described in ATHARVA-VEDA. The sutras and sub-sutras were reintroduced to the world by Swami Bharati Krishna Tirthaji Maharaja in the form of book Vedic Mathematics.

II. RELATED WORK G. Ramanjaneya Reddy and A. Srinivasulu [1] presented convolution process using hardware computing and implementations of discrete linear convolution of two finite length sequences (NXN). This implementation method is realized by simplifying the convolution building blocks. The purpose of this analysis is to prove the feasibility of an FPGA that performs a convolution on an acquired image in real time. The proposed implementation uses a changed hierarchical design approach, which efficiently and accurately quickens computation. The efficiency of the proposed convolution circuit is tested by embedding it during a prime level FPGA. It additionally provides the required modularity, expandability, and regularity to form different convolutions. This particular model has the advantage of being fine tuned for signal processing; in this case it uses the mean squared error measurement and objective measures of enhancement to achieve a more effective signal processing model. They have coded their design using the Verilog hardware description language and have synthesized it for FPGA products using ISE, Modelsim and DC compiler for other processor usage. Mohammed Hasmat Ali, Anil Kumar Sahani [2], presented the detailed study of different multipliers based on Array Multiplier, Constant coefficient multiplication (KCM) and multiplication based on vedic mathematics. Multiplicationbased operations such as Multiply and Accumulate(MAC) and inner product are among some of the frequently used Computation Intensive Arithmetic Functions(CIAF) currently implemented in many Digital Signal Processing (DSP) applications such as convolution, Fast Fourier Transform(FFT), filtering and in ALU of microprocessors. Since multiplication dominates the execution time of most DSP algorithms, so there is a need of high speed multiplier. All these multipliers are coded in Verilog HDL (Hardware Description Language) and simulated in ModelSimXEIII6.4b and synthesized in EDA tool Xilinx_ISE12.As multiplication dominates the execution time of the most Digital Signal Processing algorithms, so there is a need of high speed multiplier. The demand for high speed processing has been increasing as a result of expanding computer and signal processing applications Higher throughput arithmetic operations are important to achieve the desired performance in many real-time signal and image processing applications. One of the key arithmetic operations in such applications is multiplication and the development of fast multiplier circuit has been a subject of interest over decades. This paper presented the study of different multipliers. Madhura Tilak [3], presented a novel method of implementing linear convolution of two finite

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length sequences (N×N) in hardware using hardware description language (VHDL). In this paper, an optimized design for linear convolution is presented. This design model has advavantage of fine tuning depending on the requirement for enhancing the signal processing model. The efficiency of the proposed algorithm is tested by simulations and comparisons with different design approaches using XILLINX software. The efficiency of the proposed algorithm is tested by simulations and comparisons with different design approaches. The proposed circuit is also modular, expandable and regular which provides flexibility. The proposed system design is coded using VHDL language and synthesized for FPGA products with XILLINX 13.1 software. Abdulqadir Alaqeeli and Janusz Starzyk [4], presented substitute algorithm for calculating the convolution that requires less computation time. The algorithm uses Walsh transform instead of FFTs. FFT based algorithm requires 2 FFTs and one IFFT in addition to complex multiplications and additions. On the other hand, in the Walsh-based method the Walsh transform is required once and there is no multiplications. Therefore, using the Walsh-based algorithm can cut the processing time to about 5 percent of the required time. The additional steps in this algorithm are the permutation of the input samples and the output results. The design uses a field programmable gate array (FPGA) to apply parallel processing concept.This paper presented a design of fast convolver for CDMA signals. This is based on avoiding complex operations such as the ones in FFT-based convolvers. The substitute of the FFT is a binary transform, such as Walsh, that should reduce the operations 3 times because it uses only real additions. Surprisingly, the used algorithm does not require using the transform more than once. This made the method more efficient. The Walsh function can be transformed into a set of different phase shifts of a single PN sequence using suitable permutations. The convolution can be then performed by reordering the input sequence, performing the Walsh transform, and then permuting the output samples.

III. PROPOSED WORK

A. Convolution : Convolution is considered to be heart of the digital signal processing. It is the mathematical way of combining two signals to obtain a third signal. Convolution helps to estimate the output of a system with arbitrary input, with knowledge of impulse response of the system. Linear systems characteristics are completely specified by the systems impulse response, as governed by the mathematics of convolution. Convolution is an operation which takes two functions as input, and produces a single function output (much like addition or multiplication of functions).Consider two finite length sequences f(n) and h(n) on which the convolution operation is to be performed with lengths l and m respectively. The output of convolution operation y(n)

contains l+m-1 number of samples. The linear convolution of f(n) and h(n) is given by :

$y(n) = x(n) * h(n)$ (1)

$y[n] = \Sigma\, x(k)h(n-k) \infty\, k=-\infty$ (2)

B. Deconvolution: If the impulse response and the output of a system are known, then the procedure to obtain the unknown input is referred to as deconvolution. The concept of deconvolution is also widely used in the techniques of signal processing and image processing. In general, the object of deconvolution is to find the solution of a convolution equation of the form:

x * h = y

If the two sequences x(n) and h (n) are causal, then the convolution sum is

$y[n] = \Sigma\, x(k)h(n-k)\ n\ k=0$

Therefore, solving for x(n) given h(n) and y(n) results in

$(n) = y(n) - \Sigma\, x(k)h(n-k)\ n-1\ k=0 / h(n)$

Where (0) = y(0) / h(0)

C. Block Diagram: A block diagram of proposed system is shown in Figure 2. It consists of multiplier based on vedic sutra i.e.Urdhva-Tiryagbhyam that are embedded into convolution of two finite sequence and vedic divider that are embedded in deconvolution process to recover the original data.System block diagram is shown in Figure 2. Primary requirement of any application to work fast is that increase the speed of their basic building block. Multiplier and Divider is the heart of convolution and deconvolution respectively as shown in above fig. It is most important but, slowest unit of the system and consumes much time in the system. Many methods are invented to improve the speed of the Multiplier and Divider,

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amongst all Vedic Multiplier and Divider is under focus because, of faster working and low power consumption. In this project the speed of Convolution and Deconvolution module is improved using Vedic multiplier and Divider. It consists of multiplier based on vedic sutra i.e. URDHVA Tiryagbhyam that are embedded into convolution of two finite sequence and divider based on Vedic sutra i.e. Paravartya Sutra that are embedded in deconvolution process to recover the original data.

D. Conventional multiplier: An array multiplier is a digital combinational circuit that is used for the multiplication of two binary numbers by employing an array of full adders and half adders. This array is used for the nearly simultaneous addition of the various product terms involved.

To form the various product terms, an array of AND gates is used before the Adder array. To clarify more on the concept, let us consider a 4×4 bit multiplication with A and B being the multiplicand and the multiplier respectively. Assuming A = (1 0 0 1) and B= (1 0 1 0), the various bits of the final product can be written as:-

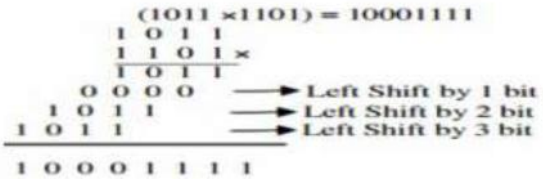

Fig.1: Example of conventional multiplier

For the above multiplication, an array of sixteen AND gates is required to form the various product terms and an Adder array is required to calculate the sums involving the various product terms and carry combinations in order to get the final Product bits. The Hardware requirement for an m x n bit array multiplier is given as:- (m x n) AND gates, (m-1).n

Adders in which n HA(Half Adders) and (m-2).n FA(full adders). Here from the above example it is inferred that partial products are generated sequentially, which reduces the speed of the multiplier. However the structure of the multiplier is regular. Also, in multiplier worst case delay would be (2n+1) td. Multiplier gives more power consumption as well as optimum number of components required, but delay for this multiplier is larger. It also requires larger number of gates because of which area is also increased; due to this multiplier is less economical.

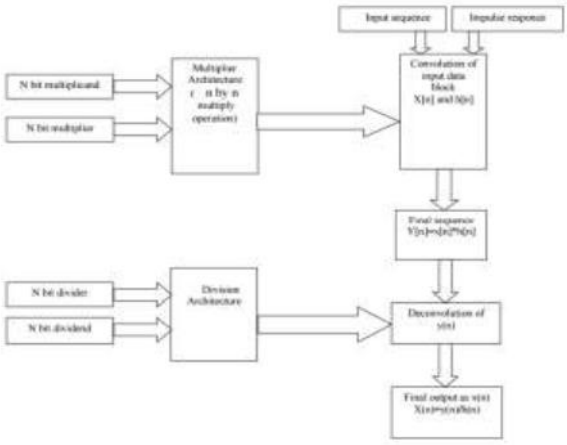

Fig.2: System Block Diagram

Consider 4x4 multiplications, say A= A3 A2 A1 A0 and B=B3 B2 B1 B0.

The output line for this multiplication is P7 P6 P5P4P3P2 P1 P0. Using the fundamental of Array Multiplication, taking partial product addition is carried out in Carry save form; we can have the following structure for multiplication as shown in Figure 3.

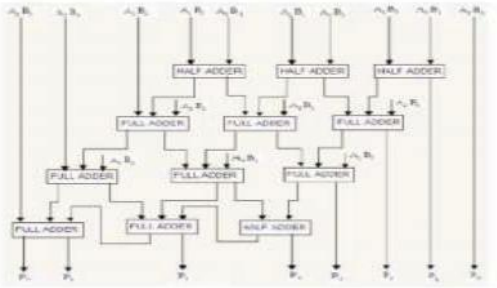

Fig.3: Structure for conventional multiplier

Urdhva Tiryagbhyam Sutra is a general multiplication formula applicable to all cases of multiplication. It literally means —Vertically and crosswise‖. It is based on a novel concept through which the generation of all partial products can be done with the concurrent addition of these partial products. Since the partial products and their sums are calculated in parallel, the multiplier is independent of the clock frequency of the processor. Thus the multiplier will require the same amount of time to calculate the product and hence is independent of the clock frequency. The net advantage is that it reduces the need of microprocessors to operate at increasingly high clock frequencies. While a higher clock frequency

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generally results in increased processing power, its disadvantage is that it also increases power dissipation which results in higher device operating temperatures. By adopting the Vedic multiplier, microprocessors designers can easily circumvent these problems to avoid catastrophic device failures.Due to its regular structure, it can be easily layout in a silicon chip. The Multiplier has the advantage that as the number of bits increases, gate delay and area increases very slowly as compared to other multipliers. Therefore it is time, space and power efficient. The main advantage of the Vedic Multiplication algorithm (Urdhva Tiryagbhyam Sutra) stems from the fact that it can be easily implemented in FPGA due to its simplicity and regularity. E. Vedic Multiplier Vedic mathematics is part of four Vedas (books of wisdom). It is part of Sthapatya-Veda (book on civil engineering and architecture), which is an upa-veda (supplement) of Atharva Veda. It gives explanation of several mathematical terms including arithmetic, geometry (plane, co-ordinate), trigonometry, quadratic equations, factorization and even calculus. His Holiness Jagadguru Shankaracharya Bharati Krishna Teerthaji Maharaja (1884- 1960) comprised all this work together and gave its mathematical explanation while discussing it for various applications. The sutras and sub-sutras were reintroduced to the world by Swami Bharati Krishna Tirthaji Maharaja in the form of book Vedic M Ancient Indian. The work presented here, makes use of Vedic Mathematics. —Urdhva Tiryagbhyam Sutra‖ or —Vertically and Crosswise Algorithm‖ of Vedic mathematics for multiplication is used to develop digital multiplier architecture. The multiplication of two 4 bit number using Urdhva Tiryagbhyam is shown in figure 4.

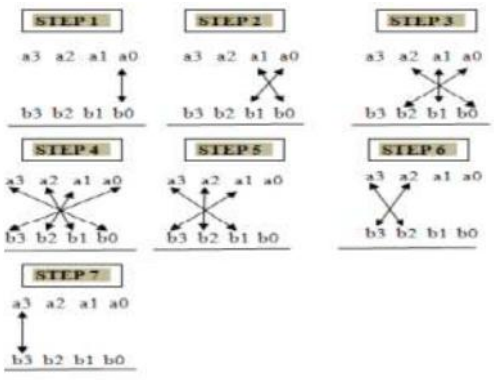

Fig.4: Multiplication of two 4 bit numbers using Urdhva Tiryagbhyam method

Thus, the product terms can be calculated as

A1=a0*b0
A2=a0*b1+a1*b0+prevcarry
A3=a0*b2+a1*b1+a2*b0+prevcarry
A4=a0*b3+a1*b2+a2*b1+a3*b0+prevcarry
A5=a1*b3+a2*b2+a3*b1+prevcarry
A6=a2*b3+a3*b2 + prevcarry
A7=a3*b3+ prevcarry

After comparative study of conventional multipliers and Vedic multiplier, Urdhva Tiryagbhyam sutra is shown to be an efficient multiplication algorithm.Therefore we are using Vedic multiplier in convolution system to improve its performance.

Proposed Deconvolution: The linear deconvolution of two finite length sequences can be solved by several method, in this approach for calculating the deconvolution ,deconvolution operation is set up like long-hand division and polynomial division ,just as the propose convolution method is similar to multiplication. In this approach division operation is implemented by using Paravartya algorithm based on Vedic mathematics while to obtain partial products Vedic multiplier is used. To illustrate the method Consider the example 2, let Y(n) be the convolved sequence equal to (8,38,77,80,49,18,3) and h(n) be the finite length sequence equal to (2,7,9,3).

IV. RESULT & DISCUSSION

This chapter presents the test environment and the experimental results of design modules. The objectives of this project are to design and implement the Vedic multiplier and divider architecture in convolution and deconvolution respectively to improve speed performance and, reduction area, power .The design is implemented in VHDL, simulated using Modelsim and synthesized by Altera Quartus II. The simulated result of Convolution using Vedic Multiplier is shown below

The analysis and synthesis of multiplier and divider is done using Altera Quartus II .Analysis shows that Vedic multiplier and divider requires less time and less power.

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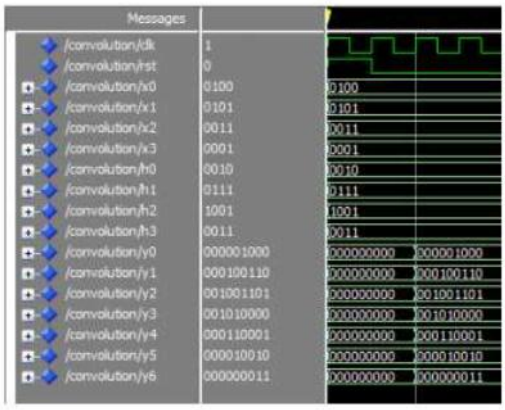

Fig.5: Simulation results of Convolution using Vedic mathematics

Table 1 shows Timming Analysis using Altera Quartus II Cyclone II for multiplier and vedic multiplier. And Table 2 shows Timming Analysis using Altera Quartus II Cyclone II for multiplier and divider. The simulated result of Deconvolution using Vedic Divider is shown below

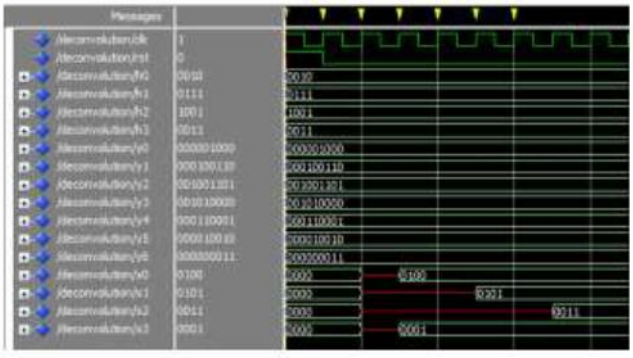

Fig.6: Simulation results of Deconvolution using Vedic mathematics

V.CONCLUSION

This propose system provides a method for calculating the linear convolution and deconvolution with the help of vedic algorithms that is easy to learn and perform.It presents faster implementation of linear convolution and deconvolution. The execution time and area required for propose convolution and deconvolution using vedic multiplication and division algorithm respectively compare with that of conventional convolution and deconvolution with the simple multiplication and division is less from the simulated result. The project, presents speedy implementation of linear convolution and deconvolution. This particular model has the advantage of being fine tuned for any signal processing application. Design is coded using the VHDL hardware description language and synthesized it for FPGA products using quartus2.

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